REMARKS

Claims 1-19 are pending in the application. Claims 1, 6, and 14-17 have been amended. Further, claims 18 and 19 are newly added to the application. No new matter has been introduced by the amendment.

Rejection Under 35 U.S.C. § 103(a)

Claims 1-11 and 15-17 have been rejected over Yoshikawa and Kawahara et al. This rejection is overcome in view of the amendment of claims 1, 6, and 15-17, together with the following remarks.

Claim 1, as amended, recites a nonvolatile semiconductor storage element that includes first and second interconnect layers. The interconnect layers electrically couple the source and drain region of the device to respective source-side and drain-side programming layers. As set forth in the Applicants' specification, by eliminating the need for separate connections to the program layer and the adjacent source or drain region, a nonvolatile, dual-bit, split-gate, storage cell can be constructed having reduced features sizes and relatively low operating voltages. (See English translation PCT application, pg. 6. lines 7-13).

A comparison of the prior art device shown in FIG. 4 of the Applicants' drawing and the embodiment of the invention illustrated in FIG. 5, shows that the device arranged in accordance with the invention reduces the number of separate electrical contacts required to operate the device. In particular, the source-side programming layer and the source region of the substrate are electrically contacted by a single source line contact (SL). Correspondingly, the drain-side programming layer and the drain region in the substrate are contacted by single bit line contact (BL).

As described in the Applicants' specification, the inventive device structure enables source side injection (SSI) and corresponding low write voltages. Further, the storage cell can be erased by avalanche conditions at relatively low erase voltages. Moreover, reverse cell read out conditions can be implemented by applying corresponding read voltages to the source side and drain side interconnect layers and to the control layer. (See English translation PCT application, pg. 7. lines 1-20; pg. 10, lines 9-25).

The Applicants' asserts that the cited references do not suggest or disclose the Applicant's innovative nonvolatile semiconductor storage element. Yoshikawa discloses a nonvolatile memory device that includes a gate contact (G) to a conductive layer (12) that overlies the gate electrode and portions of charge trapping layers (4). As acknowledged at page 3 of the instant Office Action, Yoshikawa does not teach the interconnection of the source side programming layer to the source region, and the drain side programming layer to the drain region. Instead, Yoshikawa discloses an electrical connection to the gate (3) and to the second gate electrodes (8) residing on either side of the gate (3), and separated therefrom by the charge trapping layers (4a and 4b).

Despite the failure of Yoshikawa to suggest or disclose the Applicants' innovative nonvolatile semiconductor device, the Office Action asserts that it would be obvious to construct a device having the claimed interconnect structure, because Kawahara et al. disclose an interconnect (M1a) that interconnects a select gate (SG) to the drain region (LVSD) of an adjacent transistor (LMOF). The Applicants' assert that the interconnect structure disclosed by Kawahara et al. functions to electrically couple an independent logic transistor to a nonvolatile memory cell. Accordingly, the interconnect of Kawahara et al. does not in any way function to alter the electrical contact structure of the disclosed nonvolatile memory cell (NVC), (See, for example paragraphs 0093-0098).

Kawahara et al. disclose a conventional stack-gate nonvolatile memory device in which a select gate is use to activate certain memory cells in a nonvolatile memory array. Even if the logic device interconnect structure of Kawahara et al. were somehow applied to the nonvolatile memory device of Yoshikawa et al., the combination would result in an interconnect structure for an adjacent logic transistor, and not to an interconnection of individual components within the memory cell itself.

The Applicants further assert that the device of Yoshikawa et al. does not incorporate select gate technology. Accordingly, incorporation of a select gate and the associated interconnect for separate logic devices, as taught by Kawahara et al., would change the operating principle of the Yoshikawa device. A proposed modification cannot change the principle of operation of a reference. See MPEP §2134.01 IV.

Further, a proposed modification cannot render the prior art unsatisfactory for its intended purpose. See MPEP §2134.01 V. There is simply no select gate function included in the device of Yoshikawa and, accordingly, there would be no improvement to the operation of the Yoshikawa device by including some type of select gate interconnect, such as that disclosed by Kawahara et al.

Claims 2-5 are allowable in view of their dependency from claim 1.

Claim 6 recites a method for producing a nonvolatile semiconductor storage element that includes forming a first electrically conductive interconnect layer in a first interconnect area, and a second electrically conductive interconnect layer in a second interconnect area. The electrically conductive interconnect layers reside in interconnect areas that expose the source region and the drain region and portions of the programming layers. The Applicants assert that the method recited in claim 6 is not suggested or disclosed by the cited prior art, taken alone or in combination. Neither Yoshikawa nor Kawahara et al. suggest or disclose exposing first and second interconnect areas and portions of a pattern programming layer and source and drain regions, and forming first and second electrically conductive layers therein. The Applicants' forgoing remarks with respect to the structural features of the cited references are incorporated herein.

Claims 7-11 are allowable in view of their dependence from claims 6.

Claims 15-17 have been amended to correspond to the amendment of claim 1, from which they depend. Claim 15 recites a method for writing information into the nonvolatile storage element of claim 1. In particular, voltages are applied to the first and second interconnect layers and to the control layer to generate SSI programming conditions. The voltage applied to the control layer is slightly higher than the RMS threshold voltage. The Applicants assert that the cited references fail to suggest or disclose that Applicants' method for writing information.

Claim 16 recites a method for erasing the nonvolatile semiconductor storage element of claim 1, by applying a floating potential to the first interconnect layer and a first erase voltage to the second interconnect layer. A second erase voltage, that is lower than the RMS threshold voltage, is applied to the control layer for generating an

avalanche affect condition. The Applicants assert that the recited erasing method is not suggested or disclosed at least because neither Yoshikawa nor Kawahara et al. suggest or disclose a device having the required interconnect structures to carry out the claimed erasing method.

Claim 17 recites a method for reading information from a nonvolatile semiconductor storage element of claim 1, that includes applying a first positive read voltage to the first interconnect layer, and a second read voltage to the second interconnect layer. A third read voltage is applied to the control layer for generating a reverse readout. Again, the recited reading method is facilitated by the first and second interconnect layers of the Applicants' innovative nonvolatile semiconductor storage element. These interconnect layers are not suggest or disclosed by the cited references.

Claims 12-13 have been rejected over Yoshikawa and Kawahara et al., and further in view of Liu et al.

Claim 12 depends from claim 6 and recites forming the recesses by the anisotropic dry etching of the sequence layers and by the isotropic etching back of at least the charge storage layer. Claim 13 depends from claim 12 and recites that forming a fourth insulating layer fills the charge storage layer recesses. The insulation-filled recesses function to electrically isolate the charge storage layers from the interconnect layers.

The Applicants respectfully assert that the process disclosed by Liu et al. is completely unrelated to the recess forming and insulating layer depositing process of claims 12 and 13. Liu et al. disclose a method for forming a thermal oxide layer in a substrate. In the process of Liu et al., a nitride layer is etched back from the edge of an overlying insulation layer in order to allow room for a growing thermal oxide to push past the exposed sidewalls of the charge trap layer (204).

The Applicants assert that the addition of the Liu et al. does not overcome the deficiencies of Yoshikawa and Kawahara et al. None of the cited references suggest or disclose the Applicants' method of forming interconnect layers in a non-volatile semiconductor storage element.

Claim 14 has been rejected over Yoshikawa and Kawahara et al., and further in view of Gonzalez et al. This rejection is overcome in view of the amendment of claim 1 together with the following remarks.

Claim 13, as amended, recites that forming first and second electrically conductive interconnect layers comprises depositing and planarizing a third polysilicon layer. Gonzalez et al. disclose forming a dual gate programmable read only memory cell in which electrically isolated floating gates overlie different portions of a channel region, and a control gate is capacitively coupled to the each of the two floating gates. A PBSG layer is deposited over the various gate electrodes, and source and drain contacts are then formed through the BPSG layer by depositing and planarizing polysilicon. Applicants assert that the process disclosed by Gonzalez et al. does not form openings such that source line and bit line contacts are made to source and drain regions and to programming layers, as the recited by the Applicants claims. Indeed, there is no suggestion by Gonzalez et al. that a contact opening be formed that provides an electrical interconnect to electrically couple a programming layer to an adjacent source or drain region in the substrate.

New Claims

Claims 18 and 19 are newly added to the application in order that the Applicants may more fully claim the subject matter of their invention. Claim 18 recites that the storage element of claim 1 further comprises a source line contact to the first interconnect layer. The source line is electrically connected to both the source region and the source-side programming layer. Correspondingly, claim 19 recites that the nonvolatile semiconductor storage element of claim 1 further comprises a bit line contact to the second interconnect layer. The bit line is electrically connected to both the drain region and the drain side programming layer.

Claims 18 and 19 recite an advantageous aspect of the Applicants' inventive device. Electrical connections can be provided from bit line and source line leads in a nonvolatile memory array that function to apply operating voltages to the device, such that the voltages are simultaneously applied to the source and drain regions and to the corresponding programming layers. Support for claims 18 and 19 can be found, for

example, in FIG. 5 of the Applicants' drawing, and on page 10 of the English translation of the Applicants' PCT application, lines 9-25.

The Applicants have made a novel and non-obvious contribution to the art of nonvolatile semiconductor device design and fabrication. The claims at issue distinguish over the cited references and are in condition for allowance. Accordingly, such allowance is now earnestly requested.

Respectfully submitted,

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